

ABSTRACT

The present invention is directed to an apparatus for testing a system on a chip (SOC). The apparatus comprises a first SOC comprising a first hard disk controller and a first read channel. A second SOC comprises a second hard disk controller and a second read channel, and an arbitrary waveform generator (AWG) generates a timing signal. An adder is provided in communication with the arbitrary waveform generator. The first SOC differentiates the timing signal received from the arbitrary waveform generator, and the first SOC generates a write signal in synchronization with the timing signal. The adder adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component. The second SOC differentiates the timing signal component which simulates a servo signal and the write signal component simulates a signal being accessed by a read channel.

20060108 010502